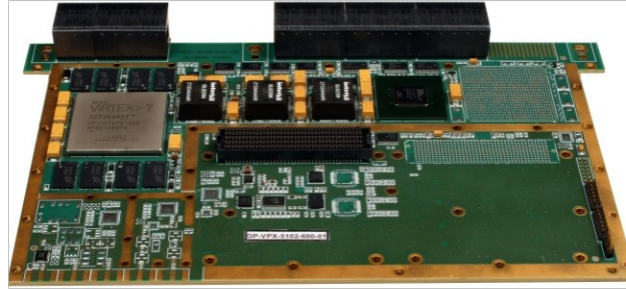


**NM-AWP-6549****DIGITAL RADIO FREQUENCY MEMORY CARD****KEY FEATURES**

- 400MHz Instantaneous Bandwidth with output attenuation control
- Pulse Widths 50 ns to CW
- Range Delay 500 ns to 500 ms
- Range Resolutions 3.33 ns
- Four numbers of 2Gbit DDR-III memory
- 4MBit flash memory
- High Speed PCIe and RIO interface
- Single Channel High speed ADC for the conversion of Analog input to Digital output with a resolution of 12 bit.
- Single Channel high speed DAC for the conversion of Digital input to Analog output with a resolution of 16 bit.
- ADC and DAC Flatness  $< \pm 2$  dBm
- User programmable Xilinx Virtex - 7 FPGA
- Output attenuation control
- External Trigger input
- External Trigger output
- External VCO input option

**APPLICATION**

- DRFM
- Radar Target Simulator
- Radar Waveform Generator
- Self-protection jamming
- Electronic warfare
- Signal Intelligence
- Radar Processing

**DESCRIPTION**

The NM-AWP-6549 (DRFM) is a VPX based standard module, which is used to measure the Amplitude, Phase & other parameters of the RADAR signal in real time using high speed ADC, DAC & FPGA architecture. DRFM digitizes an IF Signal of the intercepted radar waveform, modifies the phase/amplitude of the signal in FPGA, and coherently rebroadcasts the modified signal. DRFM effectively handles instantaneous bandwidth of 400MHz. This DRFM Card is composed of following sections,

- ADC Section
- FPGA Section
- Memory Section
- DAC Section

**ADC Section**

DRFM accepts IF analog signal as input with a single channel high speed ADC for converting IF input signal to Digital signal for further processing. The ADC used is a 12-bit monolithic sampling analog-to-digital converter (ADC) that operates at conversion rates of up to 1.2 Gsps.

**FPGA Section**

FPGA used in DRFM provides high parallel processing capabilities, reduces processor count and system size. Operations such as FFTs, FIR filters and other fixed-point and/or repetitive processing tasks are highly suited for placement inside Virtex - 7 FPGA, having 485760 logic cells and 2800 DSP Silces. The ADC and DAC is having JESD204B interface with the FPGA. One number of high speed x4 PCIe link and x4 RIO Link is from P1 connector to FPGA. ADC, DAC and Memory Interface along with the core is used to carry out user define algorithms development about 95 % of resources is available for user algorithm development.

**Memory Section**

There are four numbers of DDR3 controllers available for Virtex-7 FPGA. These DDR3 controllers are implemented inside the FPGA & interfaced with the external memory. The Data rate of each DDR3 controller is 32bit and the memory of each DDR3 controller is 2Gbit with a clock speed of 400MHz . Thus the total DDR3 memory of FPGA is 8Gbit.

**DAC Section**

DRFM is having one channel of high speed DAC for converting digital signal coming from the FPGA Section. The DAC is having a resolution of 16Bit and a sampling rate of 1.2 Gsps

**SPECIFICATIONS**

**TYPE** : 6U VPX

**IF SECTION**

No of Input Channels : 1  
 Nof of Output Channels : 1  
 IF Input frequency : 100 to 500 MHz  
 Input Impedance : 50 Ohms

**ADC SPECIFICAITON**

No of Channels : 1  
 Input Power : -50 dBm to +10dBm  
 ADC Resolution : 12 Bit ADC  
 Sampling rate : 1.2 Gsps  
 SFDR : 76dBc  
 SNR : 57.6 dBFS  
 Latency : 187 Clock Cycles  
 Interface : JESD204B

**DAC SPECIFICAITON**

No of Channels : 1  
 DAC Resolution : 16 Bit ADC  
 Sampling rate : 1.2 Gsps  
 SFDR : 67dBc  
 Interpolation : Selectable 1x - 16x  
 Digital Latency : 11 DAC Clock Cycles (No Interpolation)  
 : 83 DAC Clock Cycles (2x Interpolation)  
 Interface : JESD204B

**PERFORMANCE CHARACTERISTICS**

Instantaneous Bandwidth : 400MHz  
 Pulse Width : 50ns to CW  
 Range Delay : 500ns to 500ms  
 Range Resolution : 3.33ns  
 ADC and DAC Flatness : <±2 dBm

**FPGAAND MEMORY SPECIFICATION**

FPGA : Virtex-7  
 RAM Memory : DDR III with 400MHz Speed operating clock  
 4 memory chips of 64M x 16 Bit depth  
 Flash Memory : 4MBit (256K x 16)

**INPUT AND OUTPUT INTERFACES**

PCIe Link : One x4 PCIe link from the P1 connector to  
 Virtex-7  
 RIO Link : One x4 RIO link from the P1 connector to  
 Virtex-7

**CONNECTOR DETAILS**

SMA Connectors : IF Signals and Trigger I/O's  
 P0 : VPX Power Connector P0  
 P1 : VPX PCIe Link Interface P1  
 P2, P3, P4, P5, P6 : User defined signals

**POWER SUPPLY REQUIREMENT**

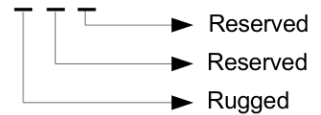
Input Voltage Nominal : +5V

**ENVIRONMENTAL SPECIFICATION**

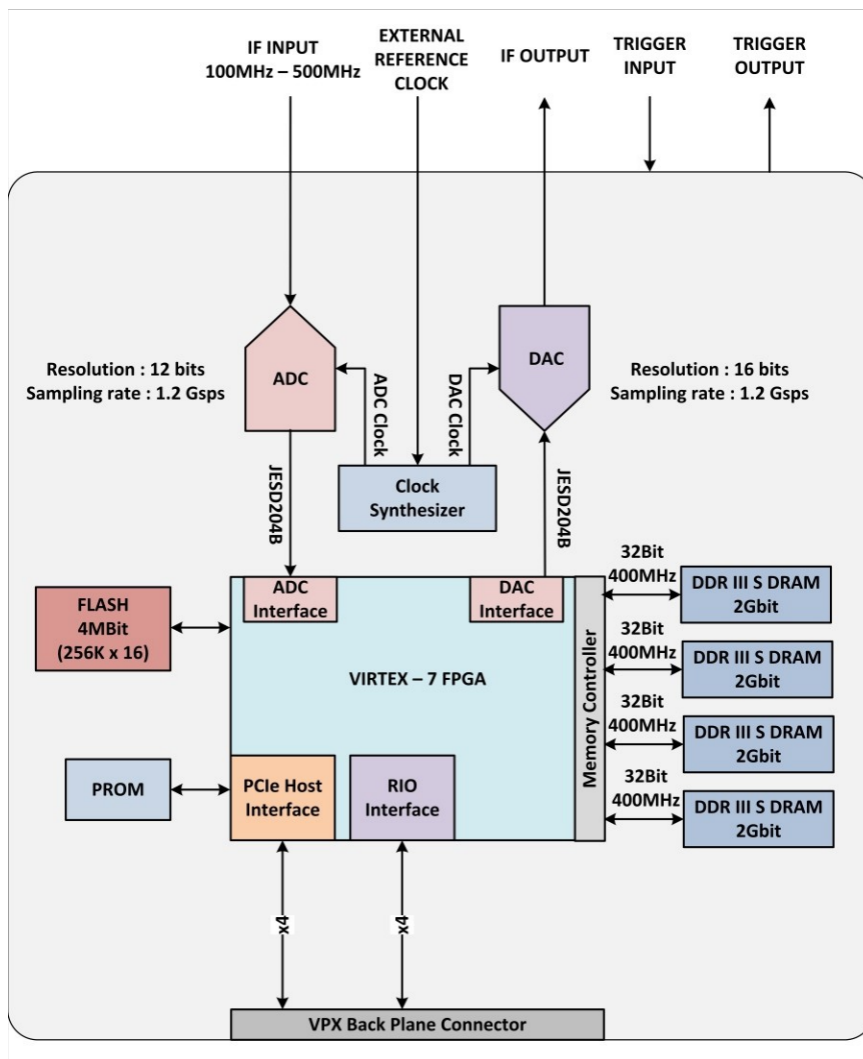
Operating Temperature : -40 deg C to +55 deg C (Typical @  
 ambient)  
 : -40 deg C to +71 deg C (Operation contact  
 factory)  
 Storage Temperature : -55 deg C to +85 deg C  
 Cooling Type : Conduction Cooled

**ORDERING INFORMATION**

NM-AWP-6549 - 6 X X



BLOCK DIAGRAM OF NM-AWP-6549



TYPICAL SYSTEM ARCHITECTURE

