

NM-EXP-7836

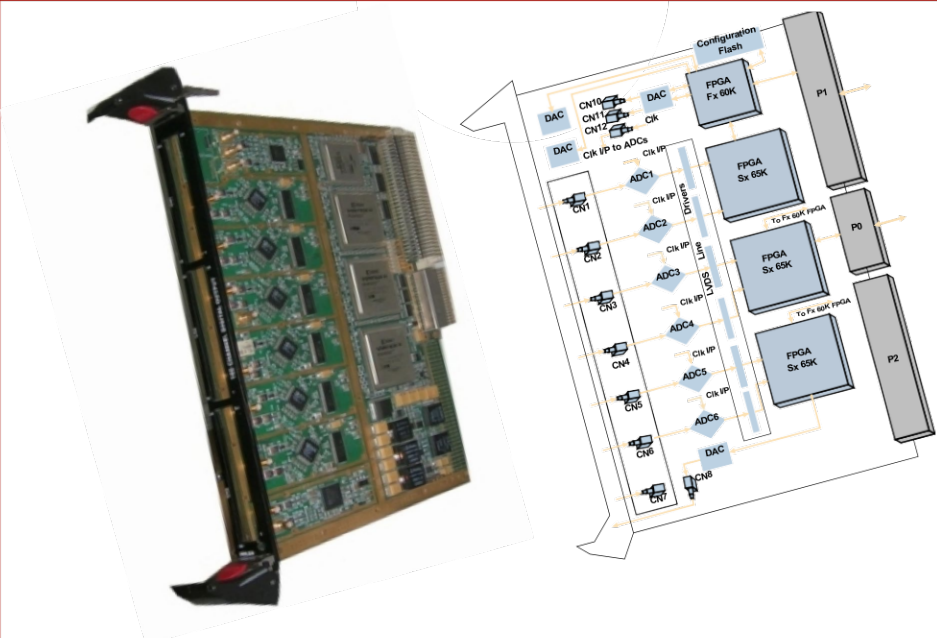
6 Channel Digital IF Receiver

KEY FEATURES AND BENEFITS

- VME 64x interface card
- High performance, monolithic 14-bit analog to digital converter
- Waveform generation DAC
- DC coupled dual channel 16-bit DACs
- Down conversion path of 6 ADCs and 3 virtex 4 FPGAs, with each 2 ADCs connected to an FPGA
- 512 MB Flash for coded waveform reference data
- 512 MB for configuration
- User programmable algorithm
- Temperature Monitoring
- Two serial Front Panel Data Ports (FPDP) optical link speed of 2.5G baud per FPDP
- Down conversion and pulse conversion
- Rugged module

APPLICATIONS

- IF signal processing
- Radar and tracking systems



DESCRIPTION

NM-EXP-7836 is a VME64x Six Channel Digital IF Receiver module. It samples and down converts analog IF signals into the digital base band data. The digital base band I/O samples generated from these IF samples are pulse compressed. Down converted I/Q data is sent to the signal processor through 2 channels of 2.5 Gbps speed SFPDP link. The digital waveform generator block of digital receiver unit generates programmable polyphase coded digital pulse coded expander output.

BLOCK LEVEL EXPLANATION

ADC

The module incorporates six 14-bit, 80MSPS/105 MSPS ADCs to convert analog signals to digital signals. These ADCs provide CMOS compatible digital outputs. These outputs are collected at the corresponding FPGAs using data ready signals from the ADC. A single field clock is given to six ADCs through a power divider. The ADC input signal and the sampling clock are terminated at 50Ω impedance in the module.

Waveform DAC

A 14-bit, 420MSPS DAC converts digital signals to analog signals. The FPGA outputs the coded data stream. A 16-bit Flash of 512 MB stores the coded waveform. Waveform generation logic is implemented using high performance DAC interface with FPGA.

Monitoring DAC

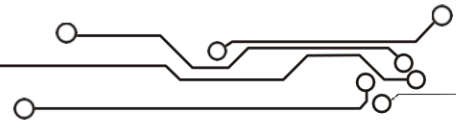
Digital receiver module incorporates a dual 16-bit DAC to monitor I & Q signals. Digital I & Q inputs are provided to dual DAC from the VME FPGA.

FPGA

The board has three virtex4 FPGAs to implement the digital down conversion and digital coded wave form generation. Each FPGA has 8 DCMs (Digital Clock Manager) and 320*18Kb RAM resource. ADC sampled data is collected at VME FPGA and processed by the user programmable algorithm. Digital processed data is given to the FPGA using the dedicated signals. This digital processed data is transmitted using SFPDP (Serial Front Panel Data Port) protocol. The optical transceiver is connected with the I/O transceiver section of virtex 4 FX FPGA. It converts electrical I & Q data into optical signals of wave length 850 nm. This board has two SFPDP channels with data rates of 2.5 Gbps.

VME Interface

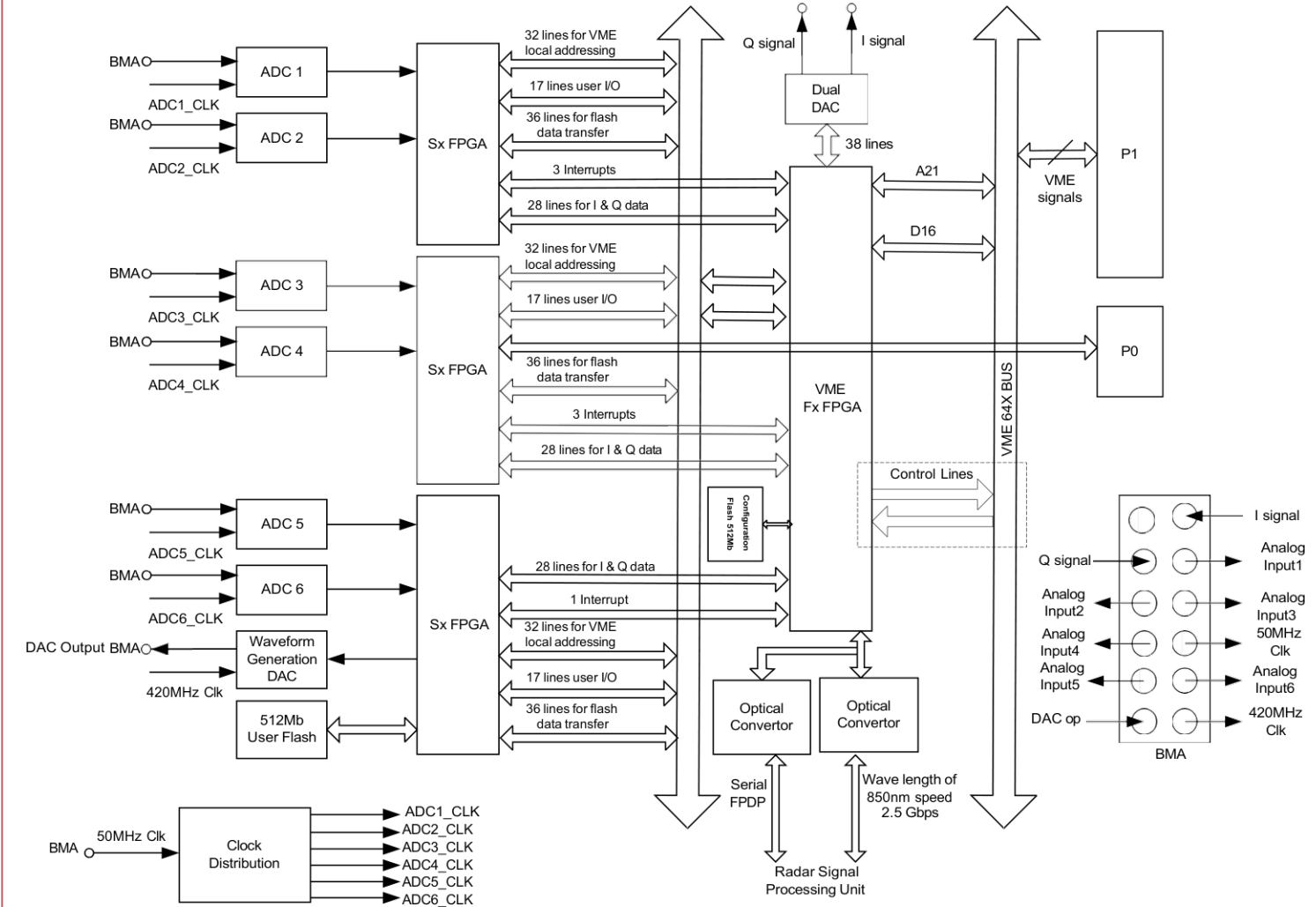
NM-EXP-7836 provides VME 64x interface which supports A24-D16 mode of operation with 6U form factor.



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SPECIFICATIONS

TYPE	: VME 6U	FPGA	
DIGITAL RECEIVER		Type	: Virtex 4-XC4VSX55
Input IF frequency	: 60MHz/120MHz	No. of FPGAs	: 3
Receiver type	: Digital down conversion	DSP slices	: 512
IF input power	: -60dBm to +10dBm	DCM per FPGA	: 8
A/D resolution	: 14 bit	Block RAM per FPGA	: 320 x 18 Kbit
D/A resolution	: 16 bit		
ANALOG INPUT		VME FPGA FX40/60	
No. of channels	: 6	No. of FPGAs	: 1
Analog input connector	: SMC receptable in board/BMA plug in module	DSP slices	: 64
Analog input termination	: Transformer coupled 50Ω	DCM per FPGA	: 8
Input frequency	: 4MHz to 120 MHz	Block RAM per FPGA	: 144 x 18 bit
Max input level	: +12dBm at 50Ω		
Resolution	: 14	WAVEFORM MEMORY (USER FLASH)	
Encoder clock bandwidth	: 2 to 80MSPS (max)/105MHz	Size	: 512 Mb
Encoder clock range	: 8dBm to 9dBm	Access Speed	: 100ns or 110ns
SNR	: ≥72dBFS		
SFDR	: ≥85dB	OPTICAL INTERFACE	
Noise floor	: ≤-110dBFS for 16K FFT	2 channel SFPDP-850nm, 2.5 Gbps, 50/125 μm cable IC optical chip	
ANALOG OUTPUT		POWER	: 5V
No. of channels	: 1	MECHANICAL	
Analog output connector	: SMC receptacle in Board/BMA plug in module	Dimension in mm (LXB)	: 233.33X160 (6U card) (Single Slot)
Input clock strength	: -4dBm at 50Ω	CONNECTOR	: VME Interface
Encoder clock frequency	: 420 MHz	SOFTWARE SUPPORT	: Vx Works 6.3
Resolution	: 14 bit	ENVIRONMENT	
Output impedance	: 50Ω	Operating temperature	: -20°C to +55°C and -40°C to +55°C
USER I/O		Storage temperature	: -40°C to 85°C and -55°C to +125°C
Output signals	: 3 TTL lines through P0 connector	ORDERING INFORMATION	
Input signals	: 14 TTL lines, 2 LVDS lines through PO connector	NM-EXP-7836-X-X-X	
I & Q MONITORING		0 - 80 MSPS	
No. of channels	: 2	1 - 105 MSPS	
Analog output connector	: SMC receptacle in board/BMA Plug in module	0 - Blind mate	
Output data	: 400 MSPS	1 - SMC connector	
Full scale O/P voltage	: 1V _{p-p}	6 - Rugged	
Resolution	: 16 bit		
Input clock	: Internal clock from FPGA		
Input clock level	: LVTTTL		



BLOCK DIAGRAM OF NM-EXP-7836

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